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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,291	03/30/2004	Richard V. Booth		4522
7590 05/25/2005 Ryan, Mason & Lewis, LLP 90 Forest Avenue Locust Valley, NY 11560			EXAMINER LE, DINH THANH	
			ART UNIT 2816	PAPER NUMBER

DATE MAILED: 05/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/813,291

Applicant(s)

RICHARG V. BOOTH

Examiner

DINH T. LE

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 3/30/04.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

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## **DETAILED ACTION**

### ***Specification***

The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### ***Claim Rejections***

#### ***Claim Rejections - 35 USC § 112***

Claims 1-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction or clarification is required.

In claim 1, it is unclear what the “designated region” on line 8 and “capacitance per unit area” on line 9 are and how the capacitance per unit area can be “optimized and the reference voltage on line 8 can be selected on line since no means for performing the selecting function is recited in the claim. The same is true for claims 2, 16-17, 20-21 and 23.

In claim 3, the recitation “the substantially constant voltage source” on line 3 lacks clear antecedent basis. The same is true for claim 4.

In claim 6, the recitation “substantially constant reference voltage” on line 2 is confusing because it is unclear if this is additional “reference voltage” or further recitation of the previously claimed “substantially constant reference voltage” on line 7 of claim 1.

In claim 16, the recitation “the variable frequency oscillator” on line 8 lacks clear antecedent basis. It is unclear where it comes from. The same is true for claim 23.

The remaining claims are dependent from the above claims and therefore also considered indefinite.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-23 are rejected under 35 USC 103 (a) as being unpatentable over Brown et al (US 6,826,246) in view of Qu (US 6,292,061) and further in view of Tam et al (US 6,828,654).

Brown et al discloses in Figure 4 a phase locked loop circuit comprising:

- a phase detector (410);
- a VCO (440); and a filter including:
- a resistive element (R);
- a capacitor (C1-C3) coupled between the filter input (VCONTROL) and a voltage source (ground); and
- a bias circuit (450, C3) coupled to the capacitor (C1) for maintaining a substantially constant reference voltage (V2) across the capacitor (C1).

However, Brown et al does not disclose that the capacitor (C1) is formed by a thick oxide MOS transistor and is biased in a designated region of operation for optimizing the first capacitance per unit area.

Qu suggests in Figure 1 a filter circuit having a transistor capacitor (36, 42) operating in linear range for reducing cost, providing good control and easily implementing on an integrated circuit, see lines 10-26.

Tam et al suggest in Figures 1-5 a filter circuit having a thin or thick oxide PMOS transistor capacitor (Figures 4-5) for reducing leakage current at low cost, see lines 35-41, column 2.

It would have been obvious to a person having skill in the art at the time the invention was made to employ the transistor capacitor as suggested by Qu and the thick MOS transistor as suggested by Tam et al in the circuit of Brown et al for the purpose of reducing cost, providing a good control and easily implementing on an integrated circuit, and reducing current leakage to stabilize the VCO output frequency. Since the modified circuit of Brown et al might be used to provide a signal source for a predetermined system, obviously, all values of the components such as resistors and capacitors should be selected to accommodate with the specification required by the system. Thus, selecting the optimum capacitance or capacitance/area of the transistor capacitors of the modified circuit of Brown et al by selecting the biased voltage is considered to be a matter of design. It would have been obvious to a person having skill in the art at the time the invention was made to select the optimum biased voltage of the transistor capacitor of the modified circuit of Brown et al for the purpose of accommodating with the

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required specification of the predetermined system. *In re Boesch*, 617F.2d272.205

USPQ215(CCPA1980).

With regard to claim 3, although Tam et al does not suggest the PMOS transistor; however, a skilled artisan realizes that the PMOS transistor can be used in the modified circuit of Brown et al since the PMOS transistor performs the same function as the NMOS transistor. Lacking of showing any criticality, selecting the oxide PMOS transistor is considered to be a matter of a design expedient for an engineer that would have been obvious at the time of the invention.

With regard to claim 4, the biased reference voltage across that transistor capacitors (CF1, CF3) of Qu is less than  $V_{DD} - V_{TH}$ , see lines 25-27, wherein the  $V_{DD}$  is supply voltage and the  $V_{TH}$  is the threshold voltage of the transistor.

With regard to claims 8 and 19, the recitation “amplifier” is read on element (450) in Figure 4 of Brown et al.

With regard to claim 10, the recitation “second capacitor” is read on the capacitor (C3) in Figure 4 of Brown et al.

With regard to claims 11-12, lacking showing any criticality, selecting the optimum capacitance value for the second capacitor is considered to be a design expedient for an engineer that would have been obvious at the time of the invention. *In re Boesch*, 617F.2d272.205 USPQ215(CCPA1980).

With regard to claim 15, employing a transistor as a resistor for easily being fabricated on an integrated circuit is well known in the art. It would have been obvious at the time the

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invention was made to employ the transistor functioned a resistor in the modified circuit of Brown et al for the purpose of implemented on an IC.

**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DINH T. LE whose telephone number is (571) 272-1745. The examiner can normally be reached on Monday-Friday (8AM-7PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY CALLAHAN can be reached at (571) 272-1740.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Dinh Le', with a long horizontal line extending to the right.

DINH LE  
Primary Examiner